

About VXI

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1. Introduction

VXIbus is a powerful open standard designed for data acquisition and Automated Test and Measurement (ATE) applications. It was originally envisioned as a replacement for rack and stack instrumentation such as GPIB. VXIbus is an acronym for VMEbus eXtensions for Instrumentation. The goal of the standard is to define a technically sound instrumentation standard based on the VMEbus that is open to all manufacturers.

The basic building blocks of a VXIbus system is a powered 13-slot *mainframe* or chassis and a wide selection of modules that implement various I/O and instrumentation related functions. The standard implements the VME backplane bus and

defines various functions to the VME uncommitted backplane pins. Crucial to Data Acquisition and ATE instrumentation applications are the extensions that provide chassis wide clocks, timing and control.

The following features illustrate the basic relationship between VME and VXI standards:

- VXI implements the VMEbus protocol for data transfers between modules.
- The VXI backplane connector is identical to VME with the same pinout for the P1 (top) connector and the center row of the P2 (bottom) connector.
- The two outer rows of the P2 connector are undefined in VME and are assigned specific functions in VXI.

1.1. VXIbus Features for Data Acquisition and ATE

The VXIbus specification provides a number of significant enhancements over VMEbus for data acquisition and ATE applications. These include:

- The VXIbus specification provides a larger (deeper) card format that increases the board real estate available to implement sophisticated analog and signal conditioning options. The deeper card provides better isolation between low-level analog signals and typically noisy digital circuitry and buses.
- The VXIbus specification includes *mandatory* analog power supply voltages and specifications for power supply noise which eliminate the need for on-board dc to dc converters to power analog circuitry as well as establishing a worst case power supply noise levels.
- The VXIbus specification provides shields on C- and D-size modules to help minimize noise pickup from adjacent modules.
- The VXIbus specification includes chassis-wide clocks and trigger lines for common clocking and triggering across modules *an important consideration when analyzing data from different modules.*
- *Geographic addressing and dynamic address allocation* is provided in the VXIbus specification. These features can be useful when modules are replaced or the system upgraded. Wiring is typically to physical slots, geographic addressing coupled with dynamic address allocation allows one to simply pull out an old module and replace it without having to set address switches. Not all VXIbus vendors provide dynamic addressing capability.
- The VXIbus specification includes cooling specifications that are crucial particularly in low-level analog applications and applications that use modules that require high power levels such as digital signal processors.

- The VXIbus specification requires that each module perform a self-test on power-up. A bit in the module status register indicates whether the module passed self-test or not.
- The VXIbus specification provides a number of *standard* registers that contain information relating to the module. These include:
 - Manufacturers ID:** Each VXIbus manufacturer is required to obtain a unique manufacturer ID that is available in this register.
 - Module ID:** An module type identifier assigned by the manufacturer ... typically the manufacturer model number.
 - Module Serial Number:** A manufacturer assigned serial number.
 - Module Hardware/Firmware Revision Level:** A manufacturer assigned revision level of the hardware and firmware.

2. VXI Module Size

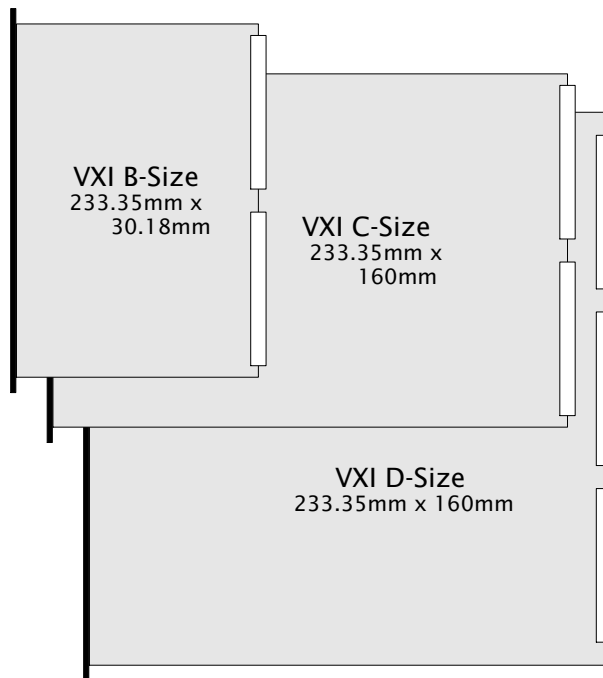


Figure 1: VXIbus Module Sizes

Three module sizes are defined by the VXIbus specification. The relative sizes are illustrated in Figure 1. The B-size is the same size as the VMEbus B-size. The

C-size which is by far the most popular and is the basis of Bustec products. It is deeper and wider than B-size VME. The extra depth provides adequate board space to implement most sophisticated instrumentation and physical isolation for low-level analog. D-size is quite large and has not found wide application. **The focus of this paper will be directed to C-size VXI.**

It is possible in some instances to mix both VXIbus and VMEbus modules, however this should only be done with great care. Some mainframes permit direct insertion of VME modules, however this only works if the VME module does not use any of the uncommitted VME pins. Inserting VME modules in a VXI backplane that use the uncommitted pins can have serious consequences due to the fact that VXI uses some pins for analog power. VME-to-VXI bus adapters do exist, but there can be side-effects due to stubs created when extending the bus due to the shorter VME card.

3. VXI Mainframe

The full-size VXIbus Mainframe is a standard 19 inch rack-mounted powered chassis that houses up to 13 VXI C- or D-size modules. Smaller mainframes are also available for C-size modules. Module positions are designated 0 through 12 left to right. The VXIbus specification covers important mainframe considerations such as cooling, power supply noise, electromagnetic compatibility (EMC) and backplane construction.

4. Slot-0 Controller

The VXIbus specification confers special status and functionality on the leftmost slot (slot-0). It includes unique backplane wiring e.g. for geographical addressing and is required to provide clock generation (10 MHz clock C- and D-size, and 100 MHz D-size). It is responsible for performing the *Resource Manager Function* at startup. In general the Slot-0 must either contain a processor its self or have a link to a processor capable of executing the resource manager function. Various implementations of the slot-0 are available including both intelligent controllers as well as controllers that are linked back to an independent computer system.

4.1. Resource Manager Function

The slot-0 is responsible for carrying out the resource manager function at power up. This includes the following:

- Identify all VXIbus devices in the mainframe.

- Manage the system self test and diagnostic sequence.
- Configure the system's A24 and A32 address maps.
- Allocate the VMEbus IRQ lines.
- Initiate normal system operation.

5. Register-based vs. Message-based Modules

The VXIbus specification provides for two backplane protocols for communicating between modules, register-based and message-based. With register-based protocol a module directly addresses the target modules' registers by placing a the register address on the VXIbus backplane and reading or writing 8-, 16- or 32-bit binary data directly to the addressed devices registers. Depending on the modules involved this transaction may be as short as 100 ns. This protocol provides by far the highest performance. *All Bustec modules use this protocol.*

Message-based protocol is a vestige of rack and stack instrumentation and GPIB. With this protocol two 8-bit ASCII characters are passed over the backplane between modules on each bus cycle. The communication is in the form of a ASCII command string which is interpreted by the receiving module and an ASCII response string is returned. With each bus cycle the sender must check whether the receiving module is ready so as not to overwhelm the receiver. This protocol is very inefficient and is only capable of using a small fraction of the VXIbus bandwidth. The single virtue is its compatibility with older instrumentation. The remainder of this paper will only deal with register-based devices.

6. VXI Extensions for C-size

The VXIbus specification for C-size includes a number of important extensions for data acquisition and ATE applications. These include:

- 10 MHz ECL System Clock $\pm 100\text{ppm}$.
- 8 TTL chassis-wide trigger lines.
- 2 ECL chassis-wide trigger lines.
- Analog SUMBUS 50 Ω summing node, current source driven.
- 12-line Local Bus propagated from slot to slot.

6.1. 10 MHz ECL System Clock

The Slot-0 Controller is responsible for generating the 10 MHz system clock. Good module design practice derives timing from this clock so that all data sampling elements within a mainframe remain in lock step.

6.2. Trigger Lines

The specification provides for 2 ECL and 8 TTL trigger lines that are available at each slot in the backplane. These lines are particularly useful for distributing clock and timing information on a chassis-wide basis. The TTL trigger lines are open collector and both the TTL and ECL trigger lines can be driven by any module in the mainframe. Three trigger line protocols are defined by the specification:

SYNC The synchronous protocol is the most commonly used. Any module can assert the trigger and one or more modules may monitor the line.

ASYNC The asynchronous protocol involves two trigger lines with a single source and single acceptor. The source initiates action by pulling the lower numbered line and the acceptor acknowledges by asserting the higher numbered line.

Start/Stop In this mode the Slot-0 drives the line and one state signifies start and the other stop.

Bustec modules make extensive use of the trigger lines and use a very flexible *trigger matrix switch* for allocating trigger lines for various module and chassis-wide functions.

6.3. Analog SUMBUS

The *Analog SUMBUS* is a 50 Ω terminated bus. Modules may drive the bus with a current source as well as monitor the sum of the currents into the 50 Ω load.

6.4. Local Bus

The *Local Bus* is a 12-line bus that is propagated from slot to slot by each module in the chain. The backplane connects LBUS-row-C pins of slot N to LBUS-row-A pins of slot N+1. A module designer chooses which set of pins to receive or send data and whether data is propagated through the module. This feature provides a convenient way of providing a private communications path between modules that form a group.

A wide range of signaling is allowed on the Local Bus by the VXIbus specification. Although not foolproof, the specification provides for keying of modules that use local bus. The objective is to minimize the chance of inserting modules that use incompatible signaling techniques in adjacent slots. Six classes are defined TTL, ECL, Analog low, medium, and high. One class is reserved.

7. Summary

The VXIbus standard incorporates a number of powerful features that can facilitate the development and on-going operation of data acquisition and ATE systems. Some of these can be particularly critical for larger systems. Features include:

Chassis-wide Clocking & Timing: Use of chassis-wide clocking and timing insures synchronous sampling between modules and facilitates comparison of data between different channels. Timing signals can be used to simultaneously start and stop data collection across multiple modules.

Manufacturer/module ID and Revision Numbers: The ability of software to read and track these parameters can be extremely useful in large systems both for maintenance purposes and validating system integrity. By recording these parameters when data is acquired it is possible to track possible causes of error when data discrepancies occur during data analysis.

Geographic Addressing: Permits validation that the correct module type is installed in the correct slot at system startup.

Dynamic Addressing: Simplifies module swapping and system configuration. This works in conjunction with geographical addressing and allows the software to dynamically assign module addresses at system startup rather than the user having to set individual module base address switches.

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